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Abstract

A high speed wide range pipelined integrator and encoder ASIC for fast digitization of charge from photomultiplier tubes is under development at Fermilab. The ASIC is intended to operate in conjunction with a FADC to digitize signals from a charge source over a dynamic range of 18-20 bits with 8-10 bits of accuracy every 16 ns. Development of the device called QIE (charge integrator and encoder) is being carried out in an IC process with CMOS and NPN devices. Many chips have been designed and tested to prove the feasibility of the device.

I. INTRODUCTION

New experiments [1] need to have a continuous record of events from which a trigger can be developed and data selected for storage. Analog pipelines have been considered for this application but the wide dynamic range needed by detectors such as PMTs and the long record lengths required by detectors with high interaction rates make such pipelines difficult to build. To solve the problem, an ASIC for integrating and digitizing detector signals in a floating point format at a very high rate has been developed. The ASIC is small, dissipates little power and in principle can be mounted in the base of a PMT along with support circuitry. Thus the signals leaving the PMT are digital and not prone to corruption, and can be recorded digitally for easy processing.

II. PRINCIPLES AND GENERAL OPERATION

The charge integrator and encoder chip receives fast wide range charge inputs and performs two functions simultaneously. One function is to scale each input signal and output an appropriate analog voltage signal to a FADC whose output forms the mantissa of the floating point number. The other function is to digitally encode the range or scale information and present that information as a four bit digital number which is the exponent of the floating point number.

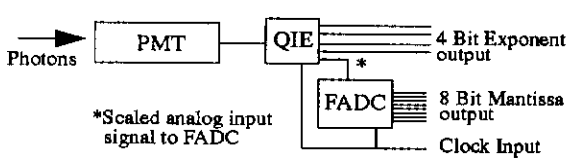

Fig 1. Simplified diagram of QIE and FADC

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Figure 1 shows the QIE chip operating with a PMT.

Processing of the analog and digital signals within the QIE are done in a four stage pipeline. Operation of the device is easily understood by looking at how the device behaves for a single input over four clock cycles. In Figure 2, consider the blocks labeled "Binary Weighted Current Splitter" and "A Bank". The charge input signal is added to a bias current and applied to the ten way binary weighted current splitter circuit. Outputs from the current splitter are simultaneously applied through current switches (SA1-SA10) to ten different capacitors of equal value for the first 16 ns clock period. S1A-S10A are then opened. The voltage which is integrated on the capacitors is largest on the I scale and decreases for each capacitor down to the I/512 scale. (Appropriate current limiting is applied where necessary to avoid overdriving the lower scales during large pulses.) The capacitor voltages are used to determine the range of the input signal by applying the capacitor voltages to a bank of comparators having a common reference voltage during the second clock period. The latched outputs of the comparators, QA1-QA10, form a digital thermometer scale. The lowest scale (I) comparator only is set for signals in the lowest range, and the other comparators also become set, in order, as the signal magnitude increases. The thermometer scale is encoded into a four bit Gray code number which is the exponent of the floating point number. During the third clock period, the latched comparator outputs are used to control a multiplexer which selects the appropriate capacitor voltage CA1-CA10 to be digitized by the FADC. The voltage which is chosen is the capacitor whose voltage lies between -1 and -2 volts. Due to the binary weighted division of the currents which are integrated on the capacitors, there can only be one capacitor voltage in this range. Digitization of the

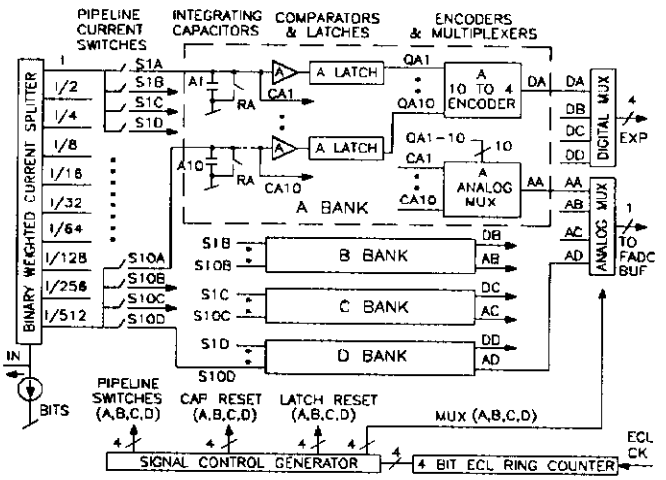

Fig. 2 Simplified block diagram of the QIE ASIC

scaled analog output by a FADC provides the 8 or 10 bit mantissa of the floating point number. During the fourth clock period, the capacitors and latches are reset.

A complete QIE has four pipelined circuit banks operating in a round robin fashion to allow integration of an input signal each 16 ns clock cycle. Each capacitor bank has its own set of comparators, latches, digital encoder, and analog multiplexer. An additional 4-way digital and 4-way analog multiplexer are required at the output of the device to sequentially select the proper analog and digital information two clock ticks after completion of the signal integration on a given capacitor bank. All of the control signals for the chip are obtained from a 4 bit ECL ring counter and CMOS signal control generator as shown at the bottom of Figure 2.

The subcircuit most critical to successful operation of the QIE chip is the binary weighted current splitter shown in Figure 2. The remainder of the QIE circuit consists of comparators, latches, encoders, multiplexers, and the control generator which, although nontrivial, are relatively straightforward to design. The current splitter is comprised of three cascaded, binary weighted, current dividers. Each divider is comprised of 8 identical NPN transistors whose collectors are connected in a binary weighted fashion (4, 2, 1, 1). The last single transistor acts as the input device for the next divider. Thus the first divider produces the I/2 to I/8 outputs, the second divider produces the I/16 to I/64 outputs, and the last divider produces the I/128 to I/512 outputs for a total of 9 scales. The I scale output is generated by a X2 multiplier circuit which applies Vbe from one of the transistors on the I/2 scale to a pair of transistors with common collectors on the I scale.

Numerous features have been added to the splitter circuit to improve performance. The first current divider is incorporated into a feedback amplifier to improve the speed and input impedance of the device. A high current bypass is built around the first divider stage to handle large input currents. Current on each output scale is arranged to pass through the same number of transistors to keep the response of each scale as uniform as possible. A bias current source is added to the input current to properly bias the feedback amplifier. Also, compensation circuits have been added to keep the bias current through each output stable with

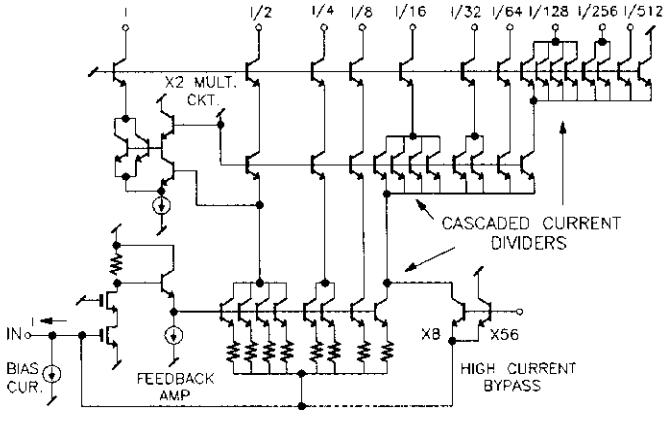

Fig. 3 Simplified binary weighted current splitter diagram

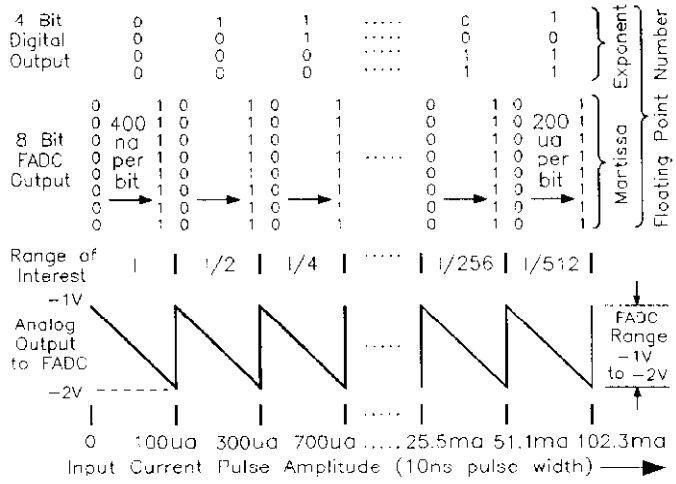

Fig. 4 Analog and digital outputs of QIE versus input current

temperature.

The bias current performs another important function. It keeps the analog signal sent to the FADC always in the same range, namely -1 to -2 volts. The DC bias current, which is nominally 62 ua, divides among the output ranges in the same way as the input signal. Figure 4 shows the analog and digital outputs for the QIE as a function of input current pulse amplitude (in the presence of the DC bias current). For no input pulse the bias current integrates to -1 V (62 ua x16 ns on 1 pf capacitor) which is output to the FADC along with a digital code of 0000. As the input signal increases, the integrated analog output voltage increases up to -2V and the FADC output increases. At -2V, the I range comparator flips, changing the digital output code to 0001 and selecting the voltage on the I/2 range capacitor for digitization. A similar process happens for the other current ranges up to 100 ma. In practice, the range of the FADC is set slightly wider than -1 to -2 V to allow for slight variations in chip processing.

III. Test Results

Many variations of two different chip sets have been designed and submitted to the Orbit 2 u "analog" process to test various performance characteristics of the QIE. One chip set has been designed to test all circuitry to the left of the comparators shown in Figure 2. The other chip set has been designed to test a full scale implementation of the remainder of the chip including the signal control generator. A complete chip combines these two chip sets into a 3 x 3 mm device.

Tests on the first chip set have shown that the splitter feedback amplifier is effective in providing good low current response and lowering the input impedance to about 40 ohms. The high current shunt around the first current divider works smoothly without any adverse affect on performance. The digital processing circuitry works well at 63 MHz.

The accuracy of the current division circuitry was measured by applying a well known current to the QIE chip input. The I/2 to I/512 outputs were measured and found to be matched in the proper ratio to better than 1%. The sum of all

the splitter output currents equaled 96% of the input current. Base currents from the four transistors in series with each output account for the missing 4%.

Integrator linearity was measured by applying an accurate variable DC input current while clocking the current switches and measuring the integrator response on the sensitive I/2 scale. In the region of interest, which is -1 to -2 V, deviation from a straight line was less than 1mv ptp. Temperature compensation circuitry is incorporated so that the integrated capacitor voltage due to the DC bias current present on each splitter output scale varies less than 1% for a 35 degree C temperature change. Nonlinearity of the I scale for the first test chip exceeded 1%. To correct the problem the current multiplier design was changed and the nonlinearity is now less than 1%.

Noise seen on the integrated capacitor output voltage is primarily set by the collector shot noise in the common base pass transistors and gate jitter on the most sensitive current scale. For the I/2 to I/512 ranges (between -1 and -2 V), the measured noise was always less than 1 mv rms. Noise on the I scale was 1.5 mv rms due to additional noise sources.

Crosstalk between a large (100 ma) current pulse on one sampling capacitor and the voltages stored on other sampling capacitors was found to be very small [2].

Capacitor mismatch, which contributes to pipeline gain variations, was found to be less than 0.5% on three chips.

Several different pulse tests have been performed on the QIE chip. A current injector, built from discrete components, was used to measure the output delay difference between current ranges. The present devices have total difference of 2 ns across all ranges, and less between adjacent ranges.

One concern is charge conservation when sampling over several capacitors. While running at 63 MHz, a narrow input current pulse was centered on one of the four sampling capacitors on the I/2 scale, then an adjacent capacitor, and then with various levels of sharing between the capacitors. An upper limit of 0.5% charge loss was measured. (Theoretically, no charge should be lost.) No measurements have been made on a multirange device.

A test board with a single range (I/2) device was built and run in the Fermilab laser test facility. A laser pulse strikes a scintillator and the resultant light output is split. A portion of the light is directed at a PMT which is connected to a QIE whose output from random sampling capacitors is digitized with a 10 bit FADC. Another portion of the scintillator light hits a linear reference photodiode whose output is also

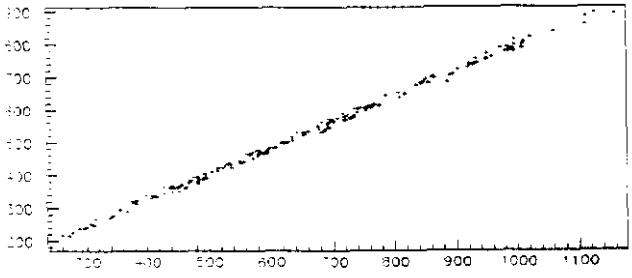

Fig. 5 QIE and FADC response versus reference diode and FADC

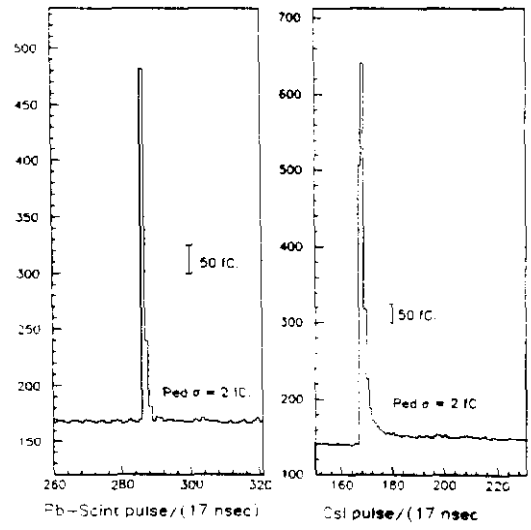

Fig. 6 PMT and scintillator response with single range QIE

digitized. The response comparing the two outputs seen in Figure 5 shows that the QIE is well behaved. The rms deviation from a straight line is 1.7% and includes capacitor mismatch, charge loss, FADC errors, and other system errors for the QIE and diode readout circuitry.

The same test board and QIE was run in a BNL test beam at 63 MHz with a PMT and two different scintillator materials. The digitized output of the QIE with a Pb glass scintillator (for use in SDC at the SSC) and a CsI crystal (for use in KTEV at Fermilab) are shown in Figure 6. In spite of the noisy beamline environment, the pedestal has an rms of only 2 fc and electron signals are easily resolved. The long tail component of the CsI is seen and the data taken with the QIE is now being used to study the time response of the CsI scintillator.

IV. CONCLUSION AND ACKNOWLEDGEMENTS

Results of the QIE tests, which have been presented, have prompted two major experiments, (SDC at SSCL, and KTEV at FNAL) to adopt the QIE for readout of their respective PMT systems. The QIE ASIC is expected to be useful in many other applications.

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V. REFERENCES

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